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Indium Gallium Zinc Oxide FinFET Compared with Silicon FinFET

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Abstract. Indium gallium zinc oxide fin-field effect transistor (IGZO FinFET) characteristics are investigated and then compared with Zinc oxide fin-field effect transistor (ZnO FinFET) and the Silicon fin-field effect transistor (Si FinFET). This was done using 3D simulation. The threshold voltage for Si, ZnO, and IGZO is 0.75 V, 0.30 V and 0.05 V respectively. The silicon device has the highest transconductance (5.0×10^{-7} S) and performs better than the other devices because it has less fixed charge defects. IGZO has the second-best value of Gm (3.6×10^{-7} S), ZnO has the least value of Gm (3.4×10^{-7} S). Si device has the least drain current (I_{DS}) value of 2.0×10^{-7} A, ZnO device has a better I_{DS} value of 6.2×10^{-6} A while IGZO device has the best I_{DS} value of 1.6×10^{-5} A. IGZO is better than Si by two (2) order magnitude. The field effect mobility is 50.0 cm^2/Vs for all three devices.

Introduction

The scaling of MOSFETs has revolutionized the semiconductor industry and enabled the realization of the immensely complex devices and systems that we rely on daily. Fin field-effect transistors (FinFETs) are derived from the metal oxide semiconductor field-effect transistors (MOSFETs) which are the devices discussed on this paper. As shown by U. Matebesi, et al., [2] MOSFETs and TFTs are devices with active regions measured in microns whereas FinFETs active regions are measured in nano-meter. Smaller transistors switch faster because they draw less current and have less capacitance which means less charge must be moved to switch the terminals on and off. The benefits of Moore's Law include increased functionality, less cost per functional reduction, and better performance [1–13]. FinFETs are fabricated along the sidewalls of a narrow, vertical fin etched surface of the wafer. That means they take up far less real estate, enabling a trillion transistors to be packed onto a chip. [6]. In these devices, the gate has more control over the channel as it is wrapped around three sides of a raised strip of silicon. This allows strong electric fields from the gate to penetrate the silicon and also increased on-currents while reducing leakage currents. The architecture of the FinFET also reduces off-state currents (I_{OFF}). The triple-gate allows for higher current drive capability [11]. The main ultimate limitation to the scaling of transistors is the atomic structure of matter which means that a MOSFET cannot be smaller than an atom [13].

In quantum mechanics, the position of an electron is not precisely defined. Therefore, with a sufficiently thin oxide layer, electrons will occasionally appear on the opposite side of the insulator. If there is an electric field, the electron will then be pulled away and unable to get back. The current through the insulator created by this phenomenon is called *tunnelling current* [11]. The fundamental quantum mechanical effects limitations to scaling are [13];

- Quantum mechanical tunnelling
- Band to Band tunnelling
- Direct gate oxide tunnelling
- Source to drain tunnelling

Scaling presents many challenges; therefore the use of alternative transistor structures has become inevitable. IGZO material has 20-50 times the electron mobility of amorphous silicon which gives it an edge when it comes to speed and resolution. The material has an added advantage of ZnO, in that it can be deposited as uniform or amorphous but continue to retain the high carrier mobility desired

for oxide semiconductors. The biggest challenge for the material is the synthesis process which is too expensive because it uses pulsed laser deposition (PLD). Currently, the material is mainly used in liquid-crystal displays (LCDs) and e-papers. This paper presents indium gallium zinc oxide field effect transistor (IGZO FinFET) as an alternative device to both the Zinc oxide fin-field effect transistor (ZnO FinFET) and the Silicon fin-field effect transistor (Si FinFET). The IGZO FinFET device overcomes the scaling and performance limitations of the Si FinFET device due to its junction-less property, whereas the IGZO FinFET has an advantage over the ZnO FinFET on performance limitations. The aim is to show that IGZO FinFET can perform just as the Si FinFET maybe even better as it is refined. The device currently does not exist in the market.

Simulation Procedure

3D Simulation is carried out using Silvaco software products. The products used are DevEdit and ATLAS. The platform uses physically-based device simulation to predict electrical characteristics associated with the specified physical structure and bias conditions. Fig. 1 shows the three (3) different structures. Table 1 lists the parameters used for the various FinFETs. The difference between the structures is the channel material which is Si or ZnO or IGZO. The Si FinFET has source and drain pads whereas the ZnO and the IGZO are junctionless. The Si FinFET is a NPN transistor with the following values: gaussian n.type concentration = 1.0 x 10^{21} cm^{-3} and p.type uniform concentration = 1.0 x 10^{18} cm^{-3}. ZnO and IGZO devices have n.type uniform concentration = 8.0 x 10^{18} cm^{-3}. The devices are unique in that they have no silicon-on-insulator (SOI) substrate when compared with the conventional MOSFET.

Table 1: Parameters used for various FinFETs simulation

No.	Physical Parameters	Si FinFET	ZnO FinFET	IGZO FinFET	Units
1	Substrate Doping	$1.32x10^{18}$	$1.32x10^{18}$	$1.32x10^{18}$	cm^{-3}
2	L = Length of channel	$0.03x10^{-6}$	$0.03x10^{-6}$	$0.03x10^{-6}$	m
3	H = Height of channel	$0.015x10^{-6}$	$0.015x10^{-6}$	$0.015x10^{-6}$	m
4	W = Width of channel	$0.015x10^{-6}$	$0.015x10^{-6}$	$0.015x10^{-6}$	m
5	SiO_2 Insulator thickness (d)	$0.05x10^{-6}$	$0.05x10^{-6}$	$10.0x10^{-9}$	m
6	Si Substrate thickness	$0.6x10^{-6}$	$0.6x10^{-6}$	$0.7x10^{-6}$	m
7	Permittivity of Chanel Material	11.9	8.12	11.9	
8	Permittivity of Oxide	3.9	3.9	3.9	

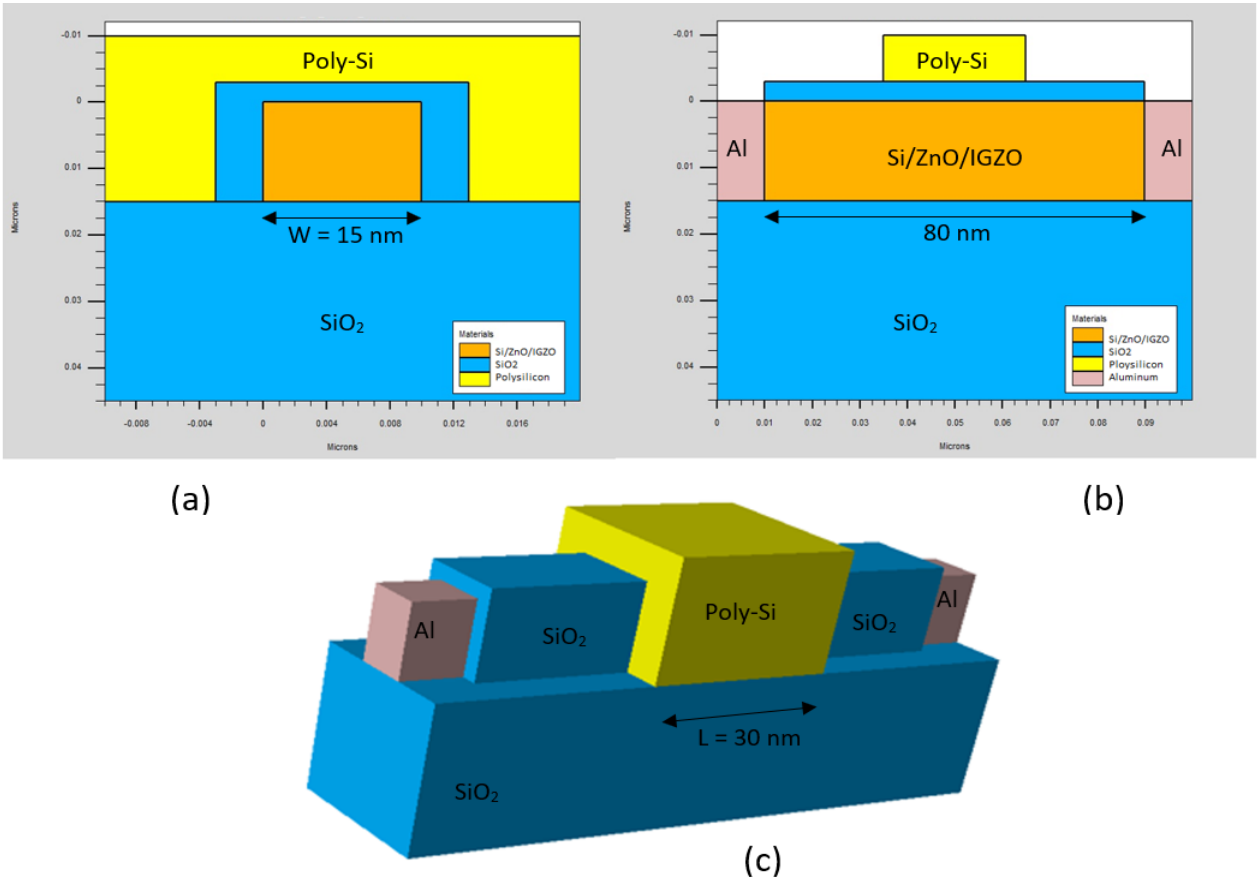

Fig. 1: Simulated devices having various material channels (Si, ZnO and IGZO) (a) 1-D plane showing the width of devices (b) 1-D plane showing the length of devices (c) 3-D plane showing devices

Table 2: The various modelling parameters used on the FinFETs

Modelling Parameter Name	Description
fermi	Fermi-Dirac: Reduced carrier concentrations in heavily doped regions (statistical approach).
bqp.n	Bohm Quantum Potential: To use the BQP model for electrons (or holes), specify BQP.N (BQP.P). Works with the Schrodinger-Poisson equation under conditions of negligible current flow.
srh	Shockley-Read-Hall recombination with fixed carrier lifetimes. Uses fixed minority carrier lifetimes.
ni.fermi	calculates n_{ie} *(*intrinsic carrier concentration*)* using Fermi-Dirac statistics.
hcte.el	Parameters enable the energy transport model for electrons only,
bqp.ngamma=$gamma	The BQP.NGAMMA and BQP.PGAMMA allow you to set the γ parameter for electrons and holes respectively.
bqp.nalpha=$alpha	BQP.NALPHA and BQP.PALPHA allow you to set the α parameter for electrons and holes respectively.
evsatmod=0	Setting EVSATMOD=0 implements, the default model for silicon based upon the Caughey-Thomas field-dependent mobility model
fldmob	Parallel Electric Field Dependence: Required to model any type of velocity saturation effect.

ATLAS has a number of modelling parameters. Table 2 lists and explains the ones used for the FinFETs. ATLAS numerical methods used are Newton and Direct. The Newton method solves the total number of unknowns for the system at the same time. It is useful when the system of equations is strongly coupled and has quadratic convergence. The downside is that the method can spend extra time solving for quantities that are essentially constant or weakly coupled. However, for almost all cases, this method is preferred, and it is the default [12]. The Gummel method solves for each unknown in turn, keeping the other variables constant and repeating the process until a stable solution is achieved. This method tolerates relatively poor initial guesses. Generally, it is useful where the system of equations is weakly coupled but has only linear convergence. It cannot be used with lumped elements or current boundary conditions [12]. The Block method solves some equations fully coupled while others are decoupled. It is useful when lattice heating or energy balance equations are included [12]. Block cannot be used in 3D simulation and Gummel is very slow to utilize.

Equations Used for 3D FinFET

The electrons in an n-type FinFET are elevated to the conduction band with the energy provided by an applied voltage V_{GS} allowing for them to move through the channel. The electrons are the majority carriers for current flow I_{DS}. The Poisson's equation plays a fundamental role in semiconductor device modelling, and by solving this system of coupled equations of the Schrödinger's equation and the Poisson's equation [6] initiates to the understanding of the relationship between the wave function and the electron density. It is one of the basic equations in electrostatics and can be derived from the Maxwell equation. Considering the three dimensions of the 3D FinFET [14], then the electrostatic potential within a 3D FinFET is determined by the non-linear Poisson's equation:

$$\frac{d^2\phi(x)}{dx^2} = \frac{q}{\varepsilon_{se}}(N_A + N_{inv}|\psi_i(x)|^2) \quad (1)$$

By considering the Fermi level, and using the Fermi-Dirac: Reduced carrier concentrations in heavily doped regions (statistical approach) model [6] then the Eigen wave function $\psi(x)$ is calculated at the lower electron energy states. Considering the surface potential $\phi(x)$, the Schrödinger's equation is solved at lower energy states.
The Schrödinger's equation is expressed as

$$\frac{-h^2}{8\pi^2 m_x}\frac{d^2\psi(x)}{dx^2} + \left(-q\phi(x)\psi(x)\right) = E_i\Psi(x) \quad (2)$$

Where h is the plank's constant $\phi(x)$ is the surface potential, $\psi(x)$ is the Eigen wave function, E_i is the lower sub-band energy, m_x is the Longitudinal effective mass

Table 3: Effective Mass

Name	Symbol	silicon	ZnO	IGZO
Longitudinal effective mass (m_x)	m_0	0.98	0.25	0.25

The solution to Schrödinger's equation for a given energy E_i involves finding the specific function $\psi(x)$ which describes that energy state [12]. The normalized wavefunction for a particle in a box is then given by the Eigen wave function expressed as

$$\Psi(x) = a_0\sqrt{\frac{2}{H}}sin\left(\frac{\pi x}{H}\right)\left[e^{\frac{-b_0 x}{H}} + e^{\frac{-b_0(H-x)}{H}}\right] \quad (3)$$

The MOSFET's basic principle of operation is that the inversion layer is formed underneath the gate to electrically connect the source and the drain. However, the electron density does not reach its maximum at the oxide-semiconductor interface but instead inside the semiconductor, while it almost vanishes right at the interface [6]. The velocity is proportional to the electric field from drain to source. V_{GS} controls the amount of inversion charge that carries the current. V_{DS} controls the electric

field that drifts the inversion charge from the source to drain [6–22]. By expanding on these principles, the model of the Inversion-Layer Centroid for the 3D FinFET taking into consideration Quantum effects can be developed. By integrating the square of the Eigen wave function $\psi(x)$, $\Psi(x)$ from $x = 0$ to $t_{ox} = \frac{H}{2}$

$$\Psi(x) = \int_{x=0}^{tox=H/2} \left(a_0 \sqrt{\frac{2}{H}} sin\left(\frac{\pi x}{H}\right) \left[e^{\frac{-b_0 x}{H}} + e^{\frac{-b_0 (H-x)}{H}} \right] \right)^2 \quad (4)$$

The Eigen wave function $\psi(x)$ is then expressed as

$$\Psi(x) = -4a_0^2 e^{-2b_0} \pi H^2 W^2 (4b_0^2 + \pi^2 + \pi^2 \, cos\, h(b_0)) + x_1 \quad (5)$$

Where x_1 is expressed as

$$x_1 = \left(\frac{\left[b_0 (b_0^2 + \pi^2) \, cosh(b_0) - (b_0^2 (3 + b_0) + (1 + b_0) \pi^2 \, sinh(b_0)) \right]}{b_0^2 HW (b_0^2 + \pi^2)^2 (4b_0^2 + \pi^2)} \right) \quad (6)$$

Where a_0 is the normalization constant expressed as

$$a_0 = \sqrt{\frac{b_0 HW (4b_0^4 + 5b_0^2 \pi^2 + \pi^4)}{8\pi HW \, sin\, h(b_0) [cos\, h(2b_0) - sinh(2b_0)] (4b_0^2 + \pi^2 + \pi^2 \, cos\, h(b_0))}} \quad (7)$$

And b_0 is the variational character

$$b_0 = (W + H)\pi^2 \left(\frac{5}{12} \frac{q^2 (m_x + n_y) Q_{inv}}{\varepsilon_{s\varepsilon} h^2} \right) \quad (8)$$

The inversion charge is calculated directly [8], in doing so obtaining an expression for the inversion charge as

$$Q(V) = 3C_{0x} \left\{ \left(\frac{-2c_{ox} v_t 2}{Q_0} \right)^2 + \sqrt{\left(\frac{2c_{Ox} v_t^2}{Q_0} \right)^2 + 4v_t^2 \, ln^2 \left[1 + exp\left(\frac{v_{gs} - v_{tn} + \Delta v_{t_h} - v}{2v_i} \right) \right]} \right\} \quad (9)$$

Where

$$Q_0 = 4 \left(\frac{kT}{q} \right) C_{se} \quad (10)$$

$$v_0 = \Delta\varphi - v_t \, ln \left(\frac{q H_{n_i}}{2Q_0} \right) \quad (11)$$

$$V_{th} = V_0 + 2v_{th} \, ln \left(1 + \frac{Q_{inv}}{2Q_0} \right) \quad (12)$$

$$\Delta V_{th} = \frac{\left(\frac{2C_{0x} v_t^2}{Q_0} \right) Q_{inv}}{\frac{Q_{inv}}{2} + Q_0} \quad (13)$$

$$C_{ox} = \frac{(\varepsilon_{ox}/t_{ox})}{1 + ((x_i/H)(\varepsilon_{ox}/t_{ox}))} \quad (14)$$

Where $v_t = kT/q$, q = electron charge, k = Boltzmann constant, T = 300 K

Taking in account the Quantum effects C_{ox} defines the FinFET's capacitance [7] by equating equation (5) and equation (9)

The Drain Current

The relationship between the drain current in the MOSFET as a function of gate-to-source voltage and drain-to-source voltage is concluded that the drain current is proportional to inversion charge and the velocity that the charge travels from source to drain [1–20]. Then for all bias conditions of the 3D FinFET in a continuous and smooth manner and taking into consideration the inversion-layer centroid model previously discussed [19], the drain current is then defined with the equation

$$I_d = \mu \frac{W}{L} \int_0^{V_{ds}} Q(V)\, dV \tag{15}$$

The drain current I_d is then obtained from,

$$I_d = \mu \frac{W}{L} \left[-2C_{ox}A + \frac{2c_{ox}(1+e_{vx})}{e_{vx}} \left(\frac{U}{2} \sqrt{A^2 + U^2} + \frac{A^2}{2} ln \left(U + \sqrt{A^2 + U^2} \right) \right) \right] \tag{16}$$

Where the values,

$$A = \frac{2C_{ox}v_t^2}{Q_0} \tag{17}$$

$$e_{vx} = e^{\frac{V_{gs} - V_{th} + \Delta V_{th} - V}{2v_t}} \tag{18}$$

$$U = 2v_t\, ln(1 + e_{vx}) \tag{19}$$

Transconductance in the MOSFET is quantified and defined as the ability of the MOSFET to amplify the signal: given by the output/input ratio, the ratio of the current change at the output port to the voltage change at the input port. The 3D FinFET's transconductance is the change in the drain current divided by the small change in the gate-source voltage with a constant drain-source voltage [18], given by

$$G_m = \frac{dI_d}{dV_{gs}} \tag{20}$$

The capacitance-voltage (CV) measurement is determined from the Inversion-Layer Centroid previously discussed, taking into account the Quantum effects, a small-signal capacitance is the slope of Q-V curve. Capacitance is linear in accumulation mode and is just due to the voltage drop across t_{ox} and is also linear in inversion, the incremental charge comes from the inversion layer because the depletion region stops growing [12]. C_v is given by

$$C_v = \frac{dQ(V)}{dV_{gs}} \tag{21}$$

Results and Discussion

Fig. 3 shows the (a) $I_{DS} - V_{DS}$ and (b) $I_{DS} - V_{GS}$ plots of the IGZO FinFET structure. It was observed that the IGZO TFT tends to operate with negative voltage based on its junctionless and n-type features. This is undesirable as it means the device is 'ON' at 0.0 V. For the device to be an effective CPU switch, it needs to operate with voltage values between 0.0 V and 5.0 V where the lower value means it is 'OFF' with no leakage currents. The threshold voltage also needs to be within 0.0 V and 0.6 V. Negative fixed charge was introduced to help turn the device 'OFF'. Fig. 3 shows that increasing the negative fixed charge from -3.0 x 10^{10} cm^{-2} to -2.0 x 10^{12} cm^{-2} slowly minimizes the leakage currents and brought the device into the desired operational voltage. This change comes with unintended consequences of decreasing the maximum currents as shown in Fig. 3(a) and degrading the subthreshold slope (shown in Fig. 3b). Fig. 3(a) shows that the pinch-off area is weak, and the saturation is inclined not flat. The quick degradation observed in the subthreshold region can also be attributed to short channel effects (SCEs). This is because SCEs tend to negatively impact the current and weaken the subthreshold slope [8]. SiO_2 is used as the dielectric material though it has lower capacitance and more thickness to avoid breakdown and leakage by quantum tunnelling [23-28]. Other dielectrics such as Al_2O_3 are more suited [23-28].

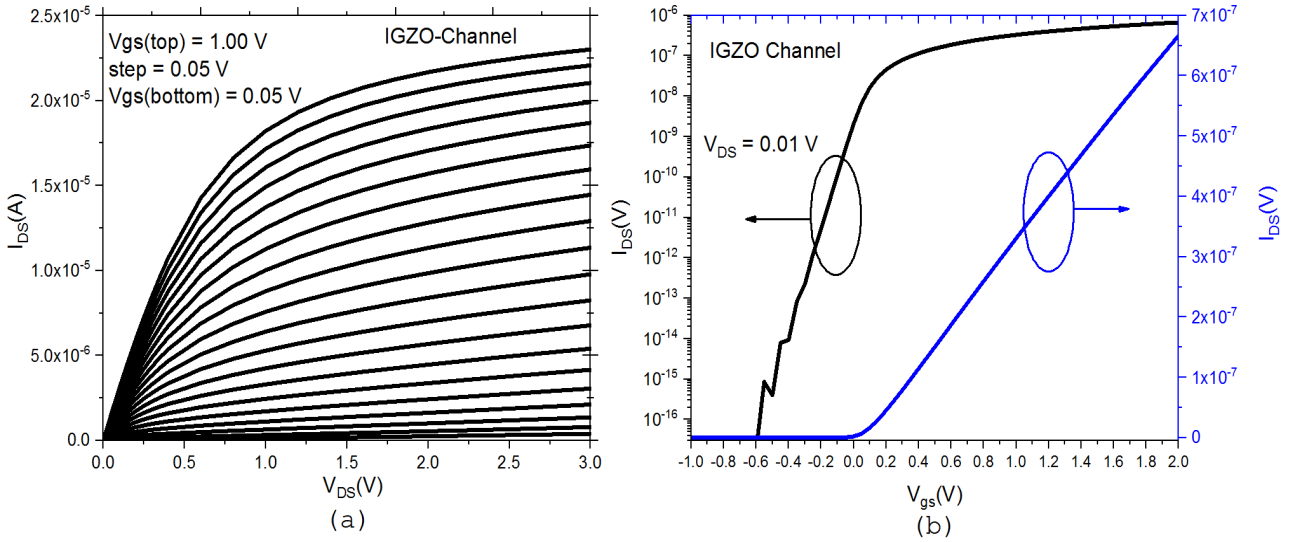

Fig. 3: (a) I_{DS}/V_{DS} for varying V_{gs} from 0.05 V to 1.00 V with steps of 0.05V (b) I_{DS}/V_{gs} Linear characteristics Subthreshold characteristics of Simulated IGZO FinFET structure

Fig. 4 shows the (a) I_{DS} – V_{GS} linear region and (b) I_{DS} – V_{GS} subthreshold region plots of the various FinFET structures. The drain voltage was kept at a value of 0.01 V for all devices. The devices are comparably competitive. Fig. 4(a) shows that the threshold voltage for Si, ZnO, and IGZO is 0.75 V, 0.30 V and 0.05 V respectively. The maximum currents are comparative at values of 6.0 x 10^{-7} A. The linear region for each device is well defined and can continue increasing at higher gate voltages without saturating. The silicon device is more aggressive compared to other devices and will saturate last. Fig. 4(b) shows that the simulation off-currents are very low at values of 10^{14} and the on/off currents are high at 10^{7} which is good. The subthreshold voltage for all the devices is roughly the same at 100 mV/decade.

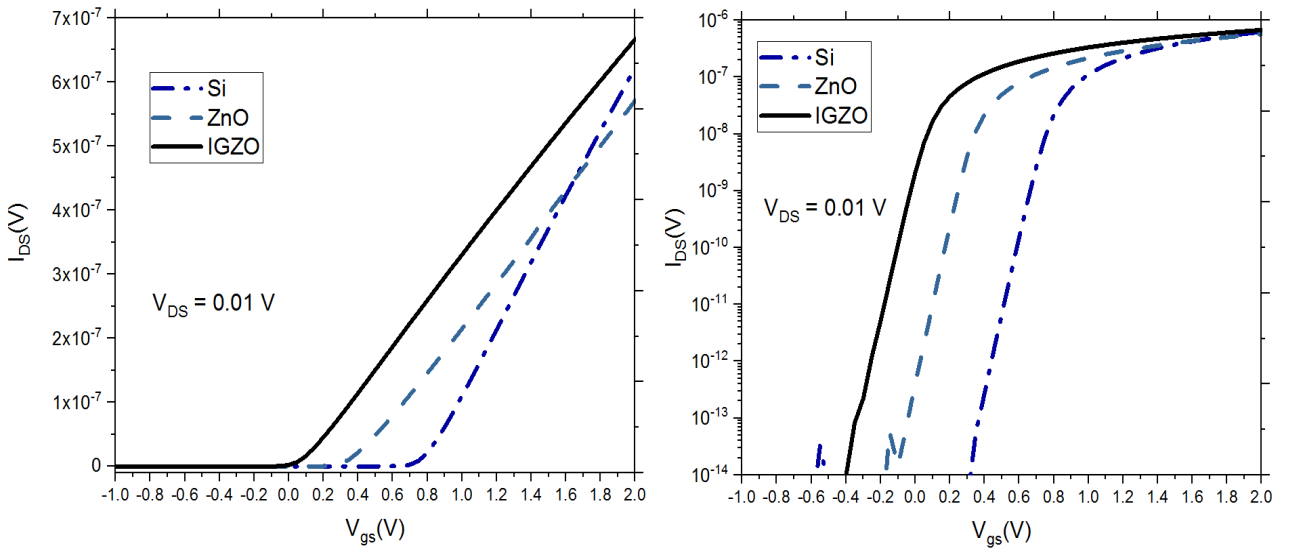

Fig. 4: A plot of drain current versus gate voltage comparing IGZO FinFET with the Si FinFET and ZnO FinFET. The graphs depict (a) in the linear region (b) in the subthreshold region

Fig. 5 shows the (a) I_{DS} – V_{DS} linear region and (b) I_{DS} – V_{DS} subthreshold region plots of the various FinFET structures. Conditions were set for all three devices: gate voltage at 0.70V and drain voltage was swept from 0.0 V to 2.0 V. IGZO device tends to outperform the other two devices with higher output currents, followed by ZnO device. Si device has the least I_{DS} value of 2.0 x 10^{-7} A, ZnO device has a better I_{DS} value of 6.2 x 10^{-6} A, IGZO device has the best I_{DS} value of 1.6 x 10^{-5} A. IGZO is better than Si by order 2. Fig. 5 shows that all the devices do not pinch-off very well and the saturation is not flat. The figure shows that devices develop flat graphs at higher drain voltages.

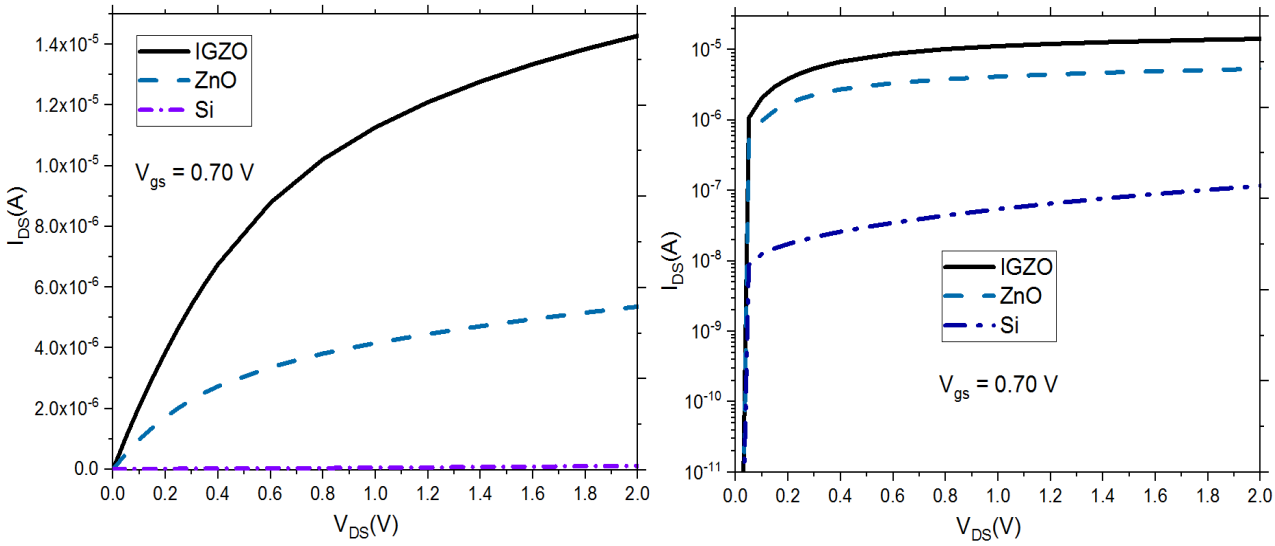

Fig. 5: A plot of drain current versus drain voltage comparing IGZO FinFET with the Si FinFET and ZnO FinFET. The graphs depict (a) in the linear region (b) in the subthreshold region

Fig. 6 shows transconductance (G(S)) verses gate voltage for all the devices. The silicon device has higher maximum transconductance (5.0 x 10^{-7} S) and performs better due to lesser fixed charge. IGZO has second best values of Gm (3.6 x 10^{-7} S), ZnO has least values of Gm (3.4 x 10^{-7} S), This is because the current difference is not large enough between the devices. The values are located at different gate voltage which is related to the threshold voltage. Field effect mobility is 50.0 cm2/Vs for all three devices.

Overall, the FinFETs attempt to overcome the worst types of short-channel effects (SCEs) encountered by the other transistors such as the MOSFETs which has a channel just below the surface. The problem is overcomed by raising the channel above the surface of the wafer thereby making it possible to wrap the gate around its three sides. The height of the FinFETs create a channel with a larger effective volume compared to MOSFETs which means This means FinFETs exhibit more drive current per unit area than MOSFETs that the devices allow for greater electrostactic control over the carriers within channel [23-28].

The devices are designed using nano-architecture via top-down processes thereby taking advantage of self-alignment to produce the extremely narrow and small features. Nanotechnology devices have been critical in moving Moore's Law further-and-further on an upward trend. The number of devices per square meter is greatly increased compared to traditional ones. Sub-0.1 mm^2 6T (6-transistor) static random-access memory (SRAMs) has been demonstrated with reasonable static noise margin (SNM) property. The optimisation of the devices produces both better voltage gain and better transconductance. MOSFET have always been developed using silicon-on-insulator (SOI) wafers, but because the channel is above the surface wafer for FinFETs, it allows for changes to be made. Bulk silicon or Glass can be used instead of SOI even though it still performs better than them [23-28].

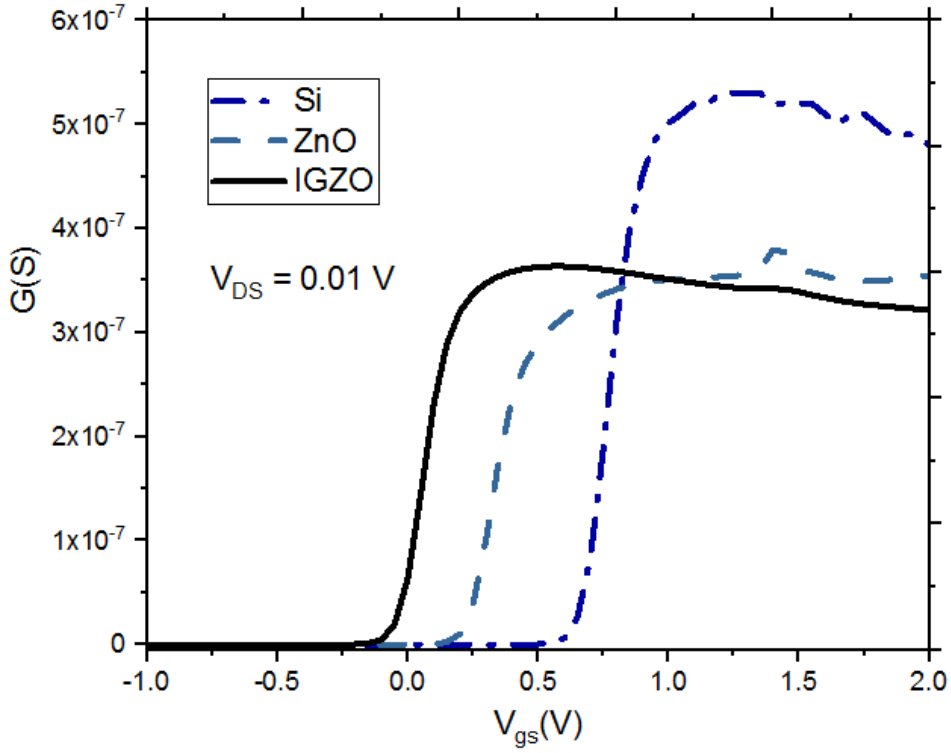

Fig. 6: Transconductance verses gate voltage. The silicon device has higher maximum transconductance and performs better due to lesser fixed charge

Conclusion

FinFETs show clear advantages in SCEs control and device variability when compared to MOSFETs. The advantages of nanotechnology used allows for scaled SRAM and analog circuit applications. Sub-0.1 mm2 6T SRAMs have been demonstrated with excellent SNM properties. Optimised FinFETs produce better voltage gain and better transconductance. Indium gallium zinc oxide fin-field effect transistor (IGZO FinFET) characteristics were compared with Zinc oxide fin-field effect transistor (ZnO FinFET) and the Silicon fin-field effect transistor (Si FinFET). The threshold voltage for Si, ZnO, and IGZOis 0.75 V, 0.30 V and 0.05 V respectively. The silicon device has the highest transconductance (5.0 x 10^{-7} S) and performs better due to the lesser fixed charge. IGZO has the second best values of Gm (3.6 x 10^{-7} S), ZnO has the least values of Gm (3.4 x 10^{-7} S). Si device has the least drain current (I_{DS}) value of 2.0 x 10^{-7} A, ZnO device has a better I_{DS} value of 6.2 x 10^{-6} A, IGZO device has the best I_{DS} value of 1.6 x 10^{-5} A. IGZO is better than Si by order 2. Field effect mobility is 50.0 cm2/Vs for all three devices.

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